Fig. 1 PRIOR ART

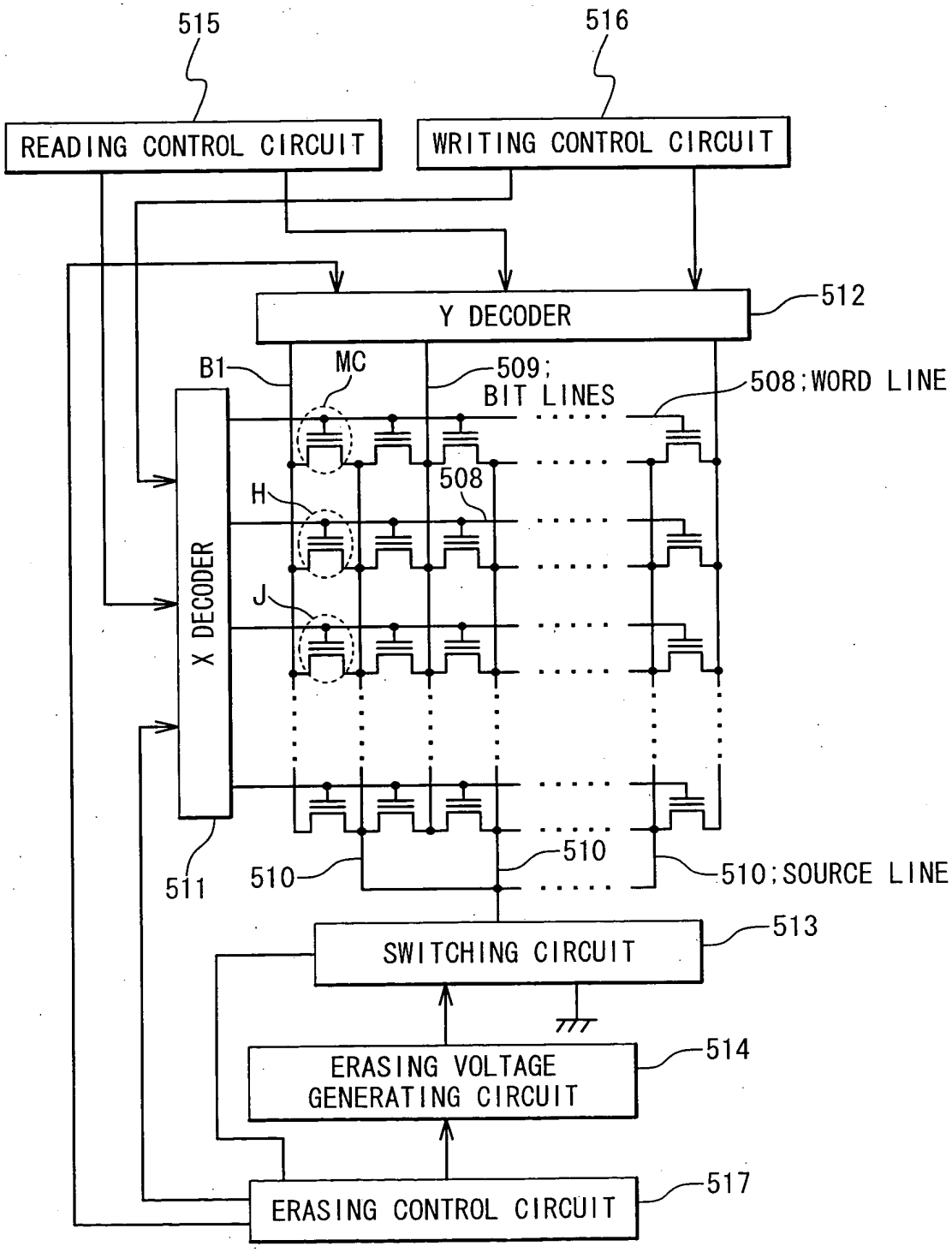


Fig. 2A PRIOR ART

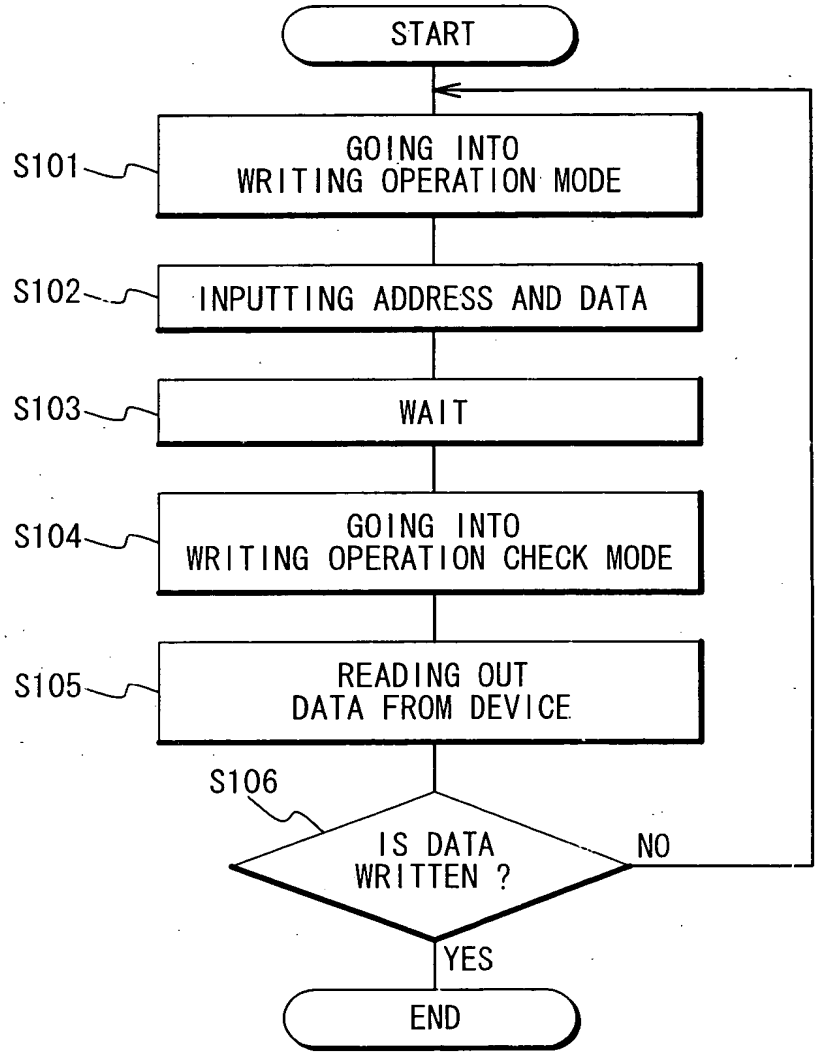


Fig. 2B PRIOR ART

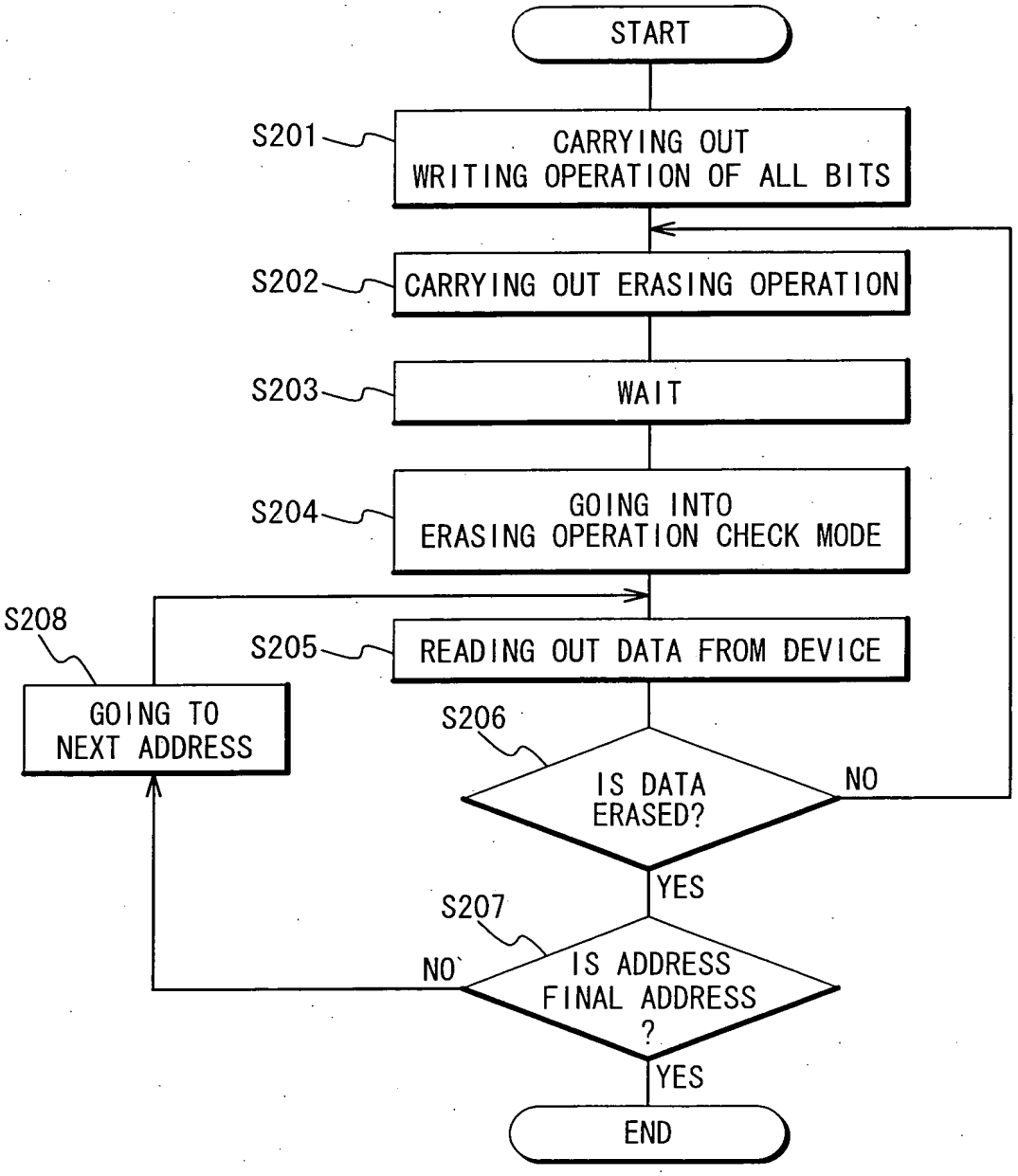


Fig. 3 PRIOR ART

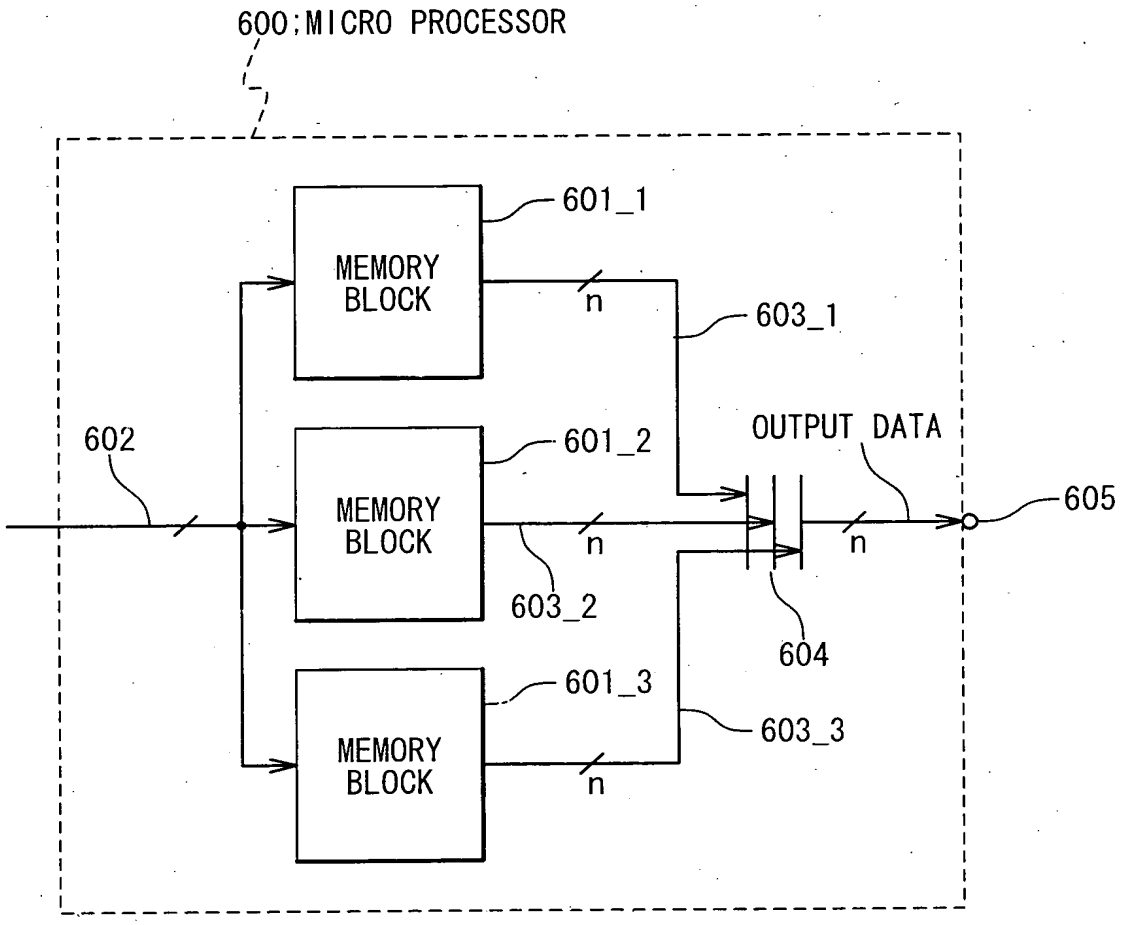


Fig. 4 PRIOR ART

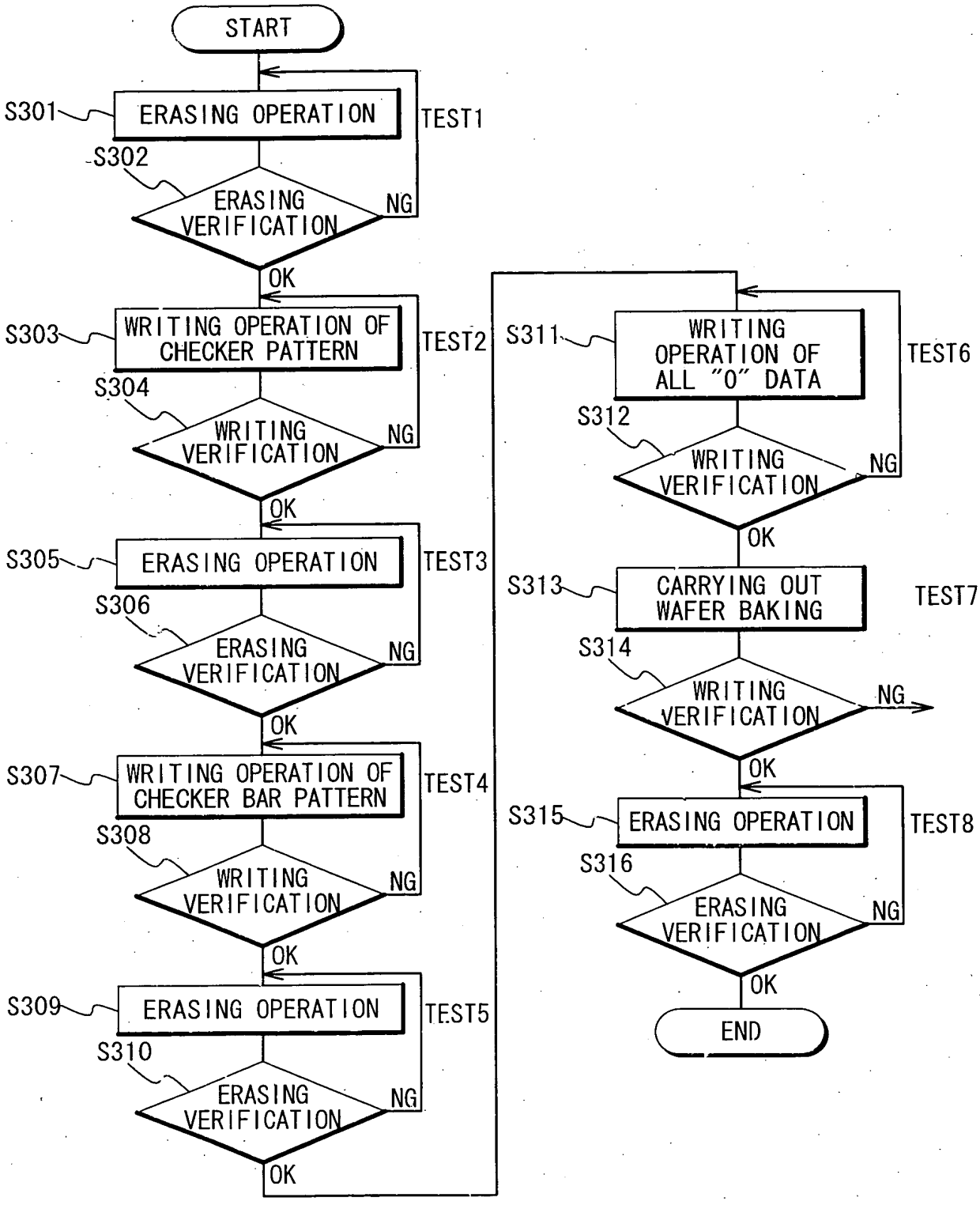


Fig. 5A PRIOR ART

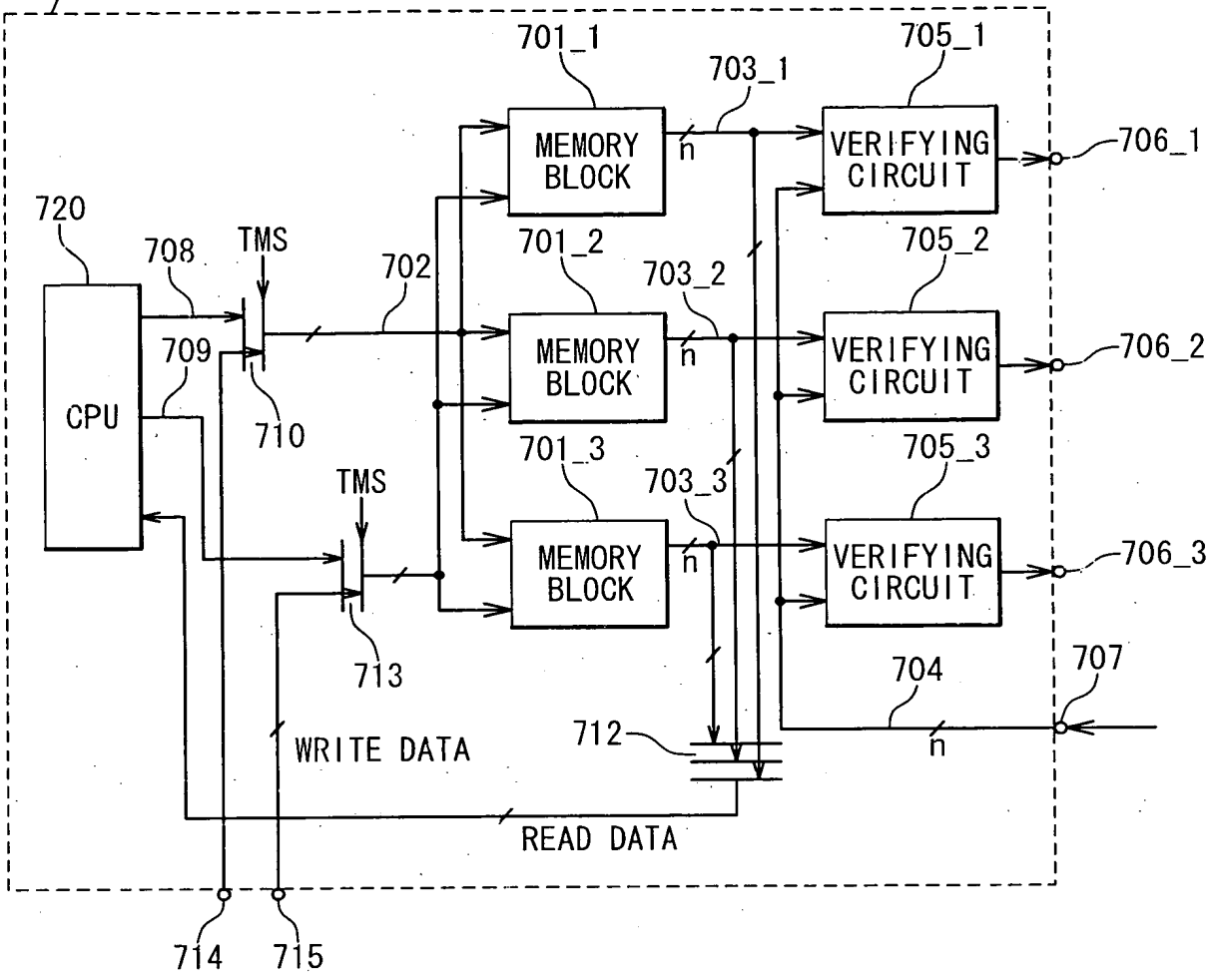


Fig. 5B PRIOR ART

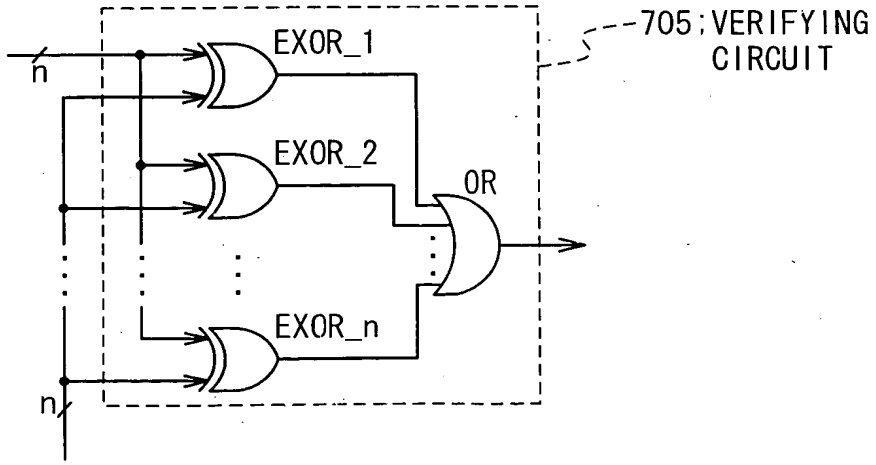


Fig. 6A

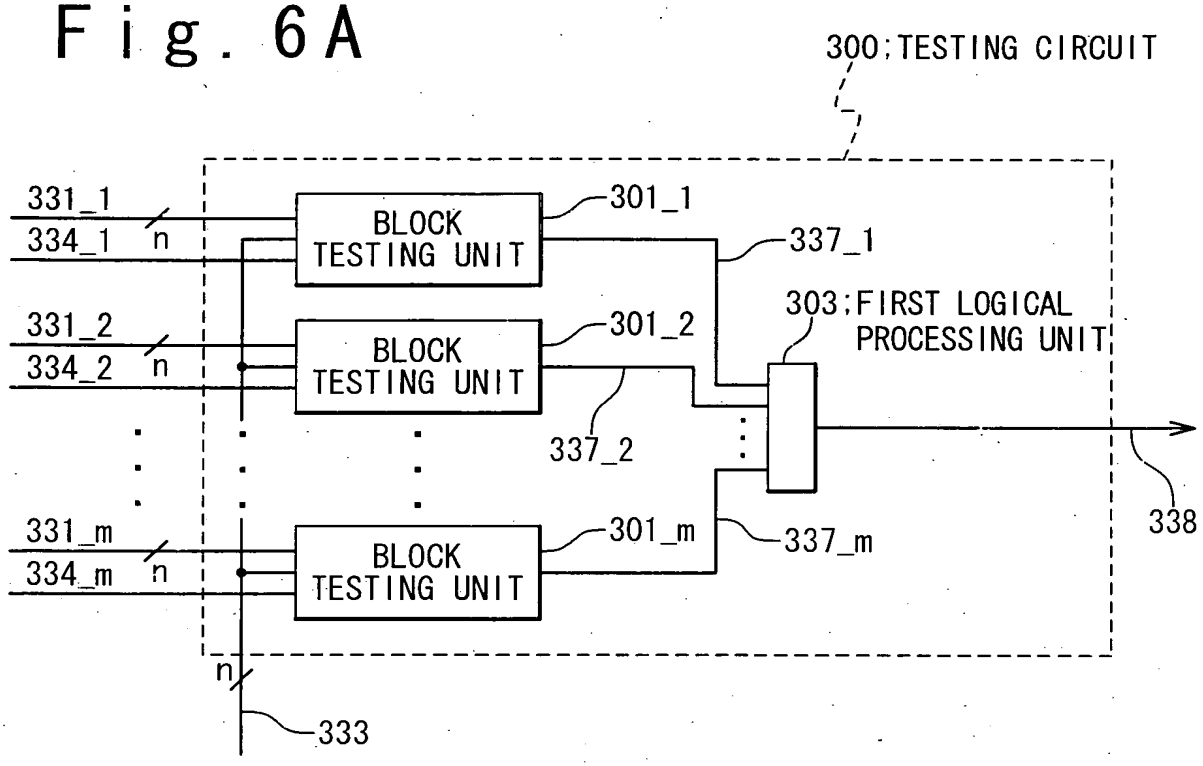

300;TESTING CIRCUIT
331_1
334_1
n
BLOCK TESTING UNIT
301_1
337_1
303;FIRST LOGICAL PROCESSING UNIT
331_2
334_2
n
BLOCK TESTING UNIT
301_2
337_2
338
331_m
334_m
n
BLOCK TESTING UNIT
301_m
337_m
n
333

Fig. 6B

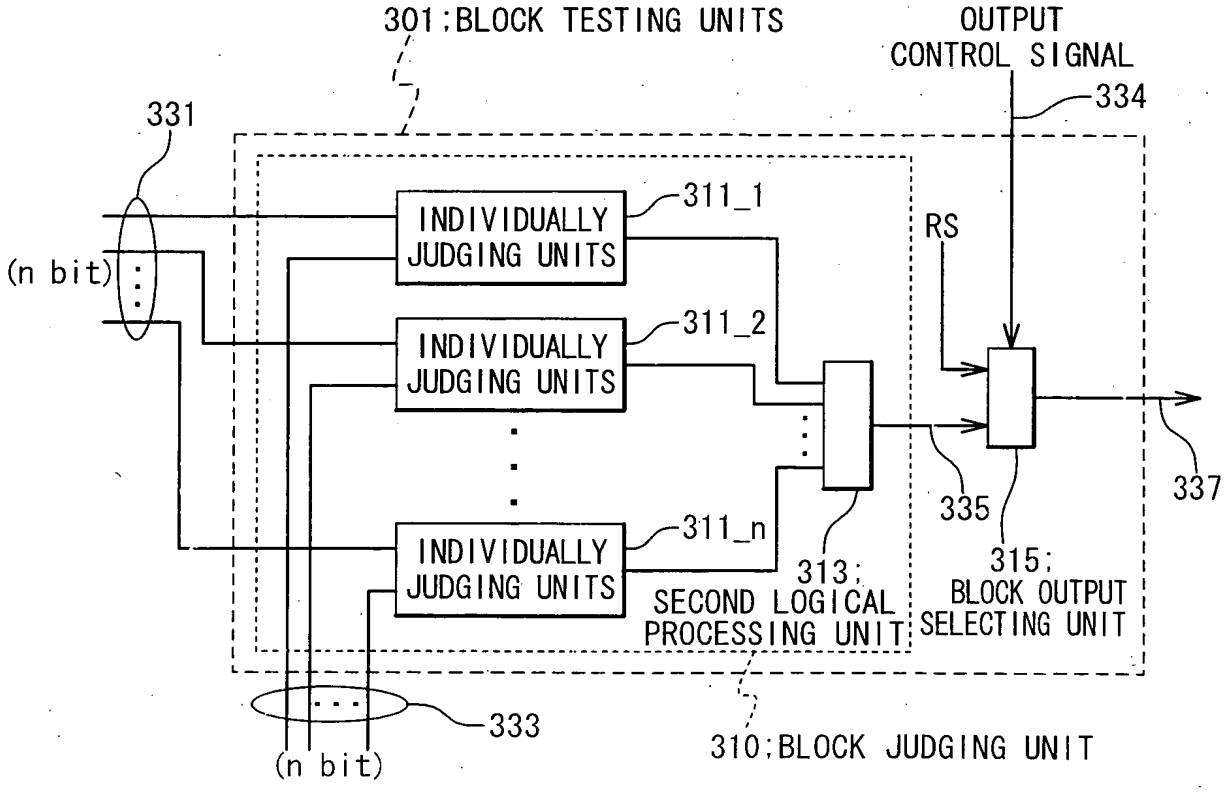

301;BLOCK TESTING UNITS
OUTPUT CONTROL SIGNAL
334
331
(n bit)
INDIVIDUALLY JUDGING UNITS
311_1
INDIVIDUALLY JUDGING UNITS
311_2
INDIVIDUALLY JUDGING UNITS
311_n
RS
335
337
313;
SECOND LOGICAL PROCESSING UNIT
315;
BLOCK OUTPUT SELECTING UNIT
333
(n bit)
310;BLOCK JUDGING UNIT

Fig. 7

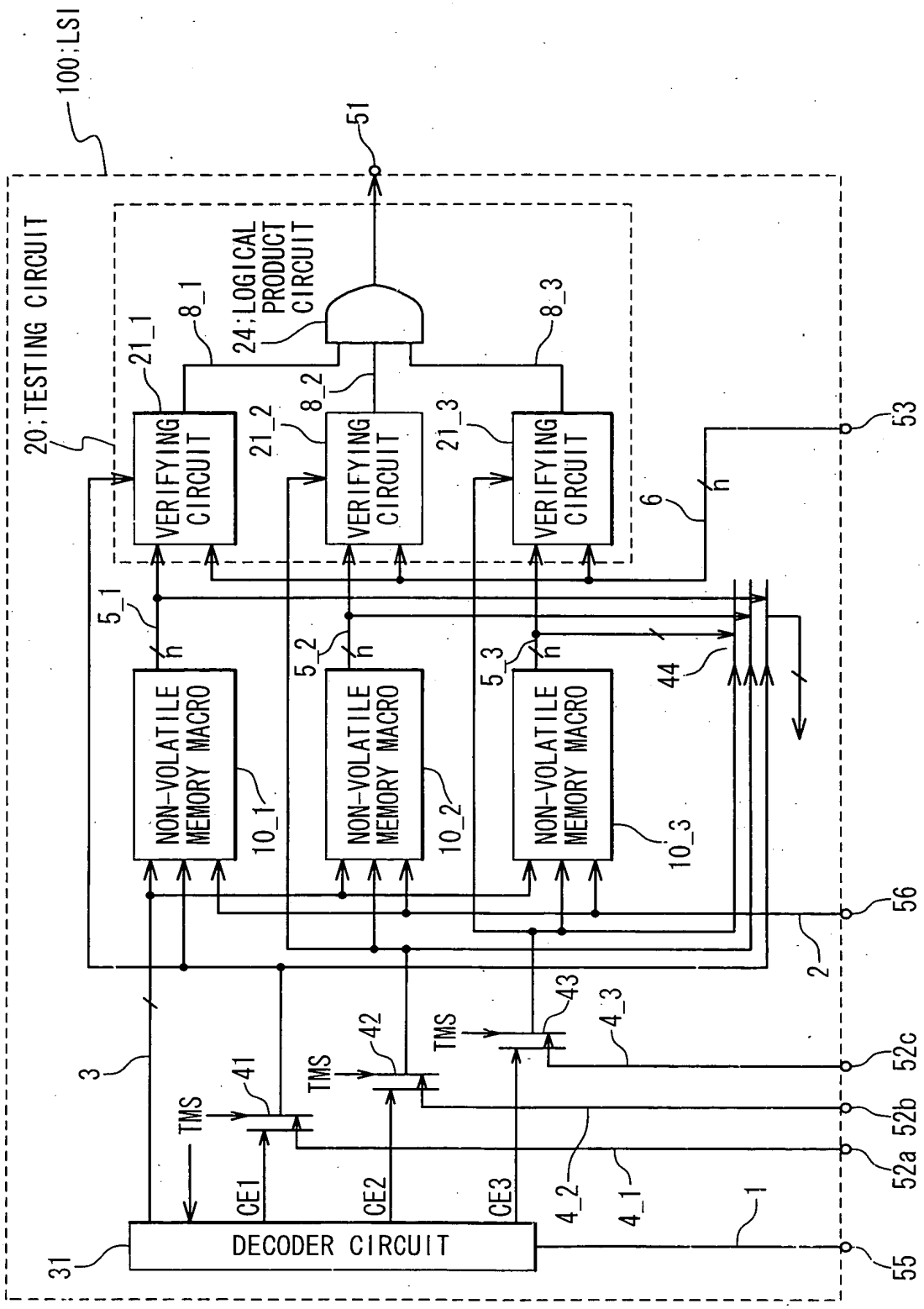

100:LSI
20:TESTING CIRCUIT
24:LOGICAL PRODUCT CIRCUIT
51
8_1
8_2
8_3
21_1
21_2
21_3
VERIFYING CIRCUIT
VERIFYING CIRCUIT
VERIFYING CIRCUIT
53
6
h
5_1
5_2
5_3
44
NON-VOLATILE MEMORY MACRO
NON-VOLATILE MEMORY MACRO
NON-VOLATILE MEMORY MACRO
10_1
10_2
10_3
56
2
3
43
4_3
42
41
TMS
TMS
TMS
52c
52b
52a
CE1
CE2
CE3
4_2
4_1
1
DECODER CIRCUIT
31
55

Fig. 8

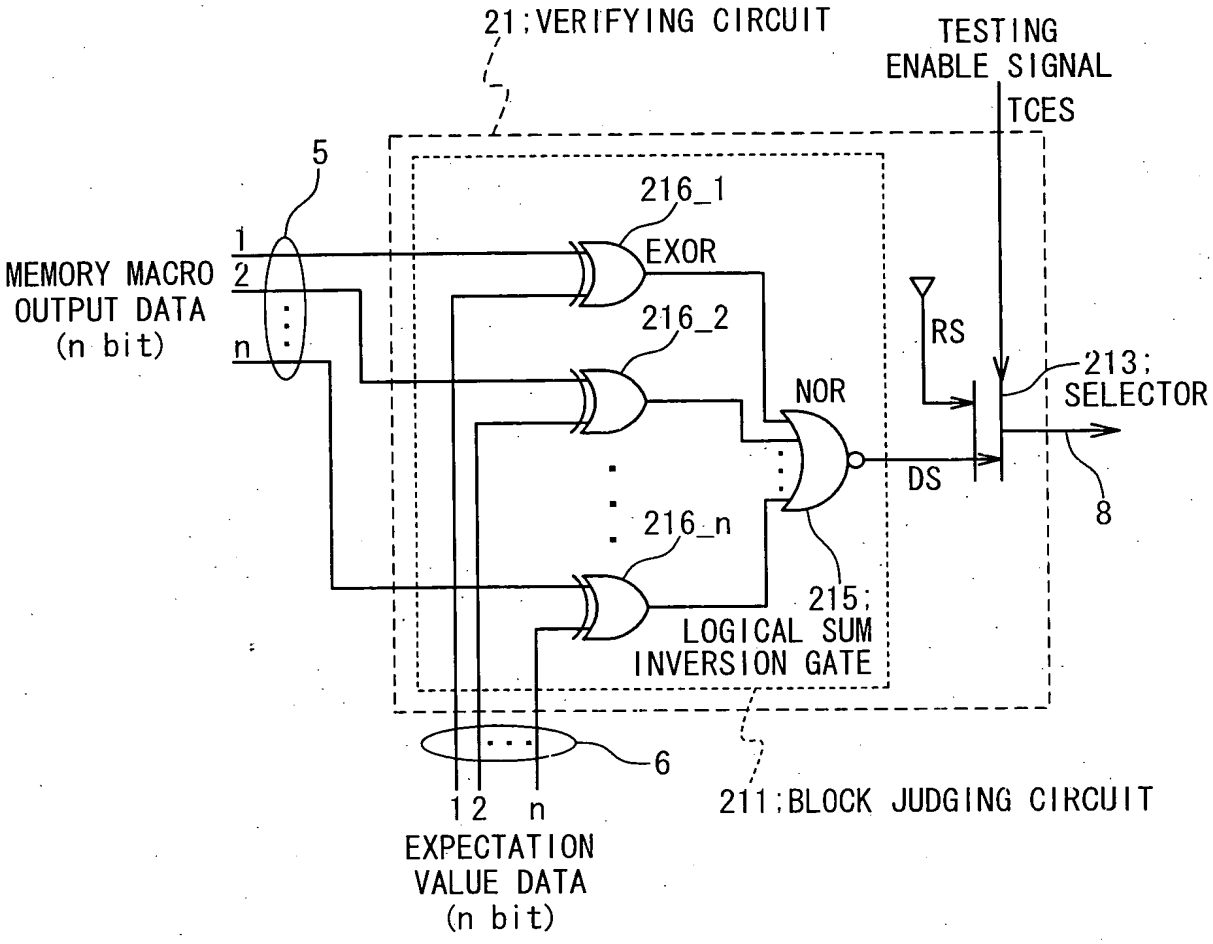

21;VERIFYING CIRCUIT
TESTING ENABLE SIGNAL
TCES
5
MEMORY MACRO OUTPUT DATA (n bit)
1
2
n
216_1
EXOR
216_2
NOR
RS
213; SELECTOR
DS
8
216_n
215; LOGICAL SUM INVERSION GATE
6
1 2 n
EXPECTATION VALUE DATA (n bit)
211;BLOCK JUDGING CIRCUIT

Fig. 9A

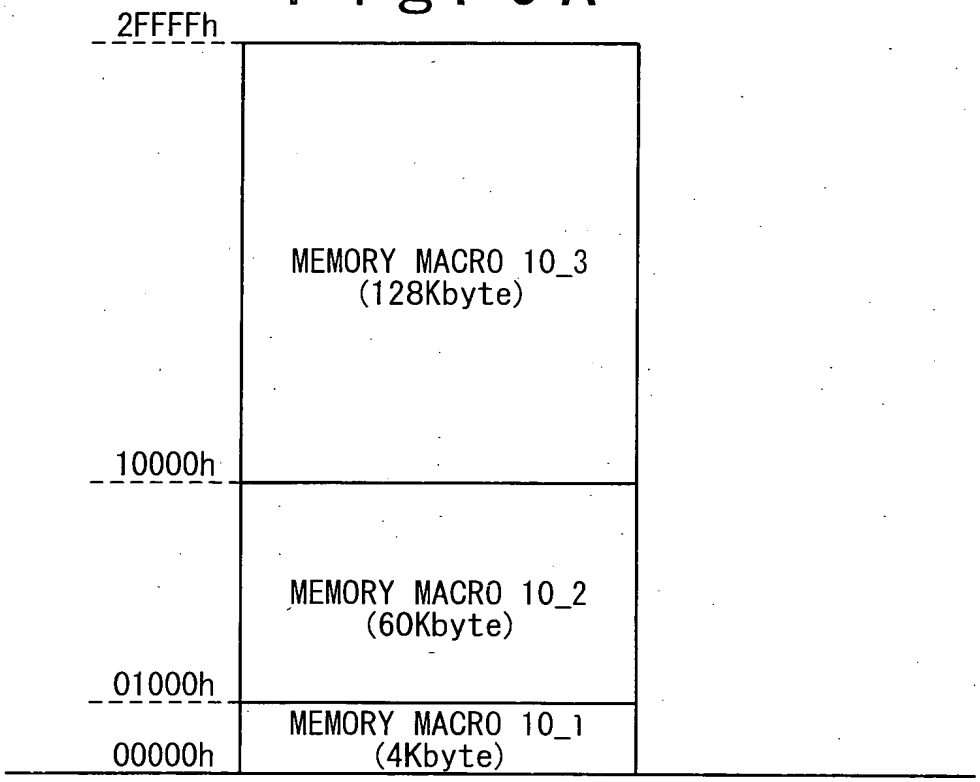


Fig. 9B

		FIRST SECOND	OUTPUT OF DECODE CIRCUIT			
			CE3	CE2	CE1	SECOND ADDRESS
MEMORY MACRO 10_3	FINAL ADDRESS START ADDRESS	2FFFFh ~ 10000h	1	0	0	1FFFFh ~ 00000h
MEMORY MACRO 10_2	FINAL ADDRESS START ADDRESS	0FFFFh ~ 01000h	0	1	0	0EFFFh ~ 00000h
MEMORY MACRO 10_1	FINAL ADDRESS START ADDRESS	00FFFh ~ 00000h	0	0	1	00FFFh ~ 00000h

Fig. 10A

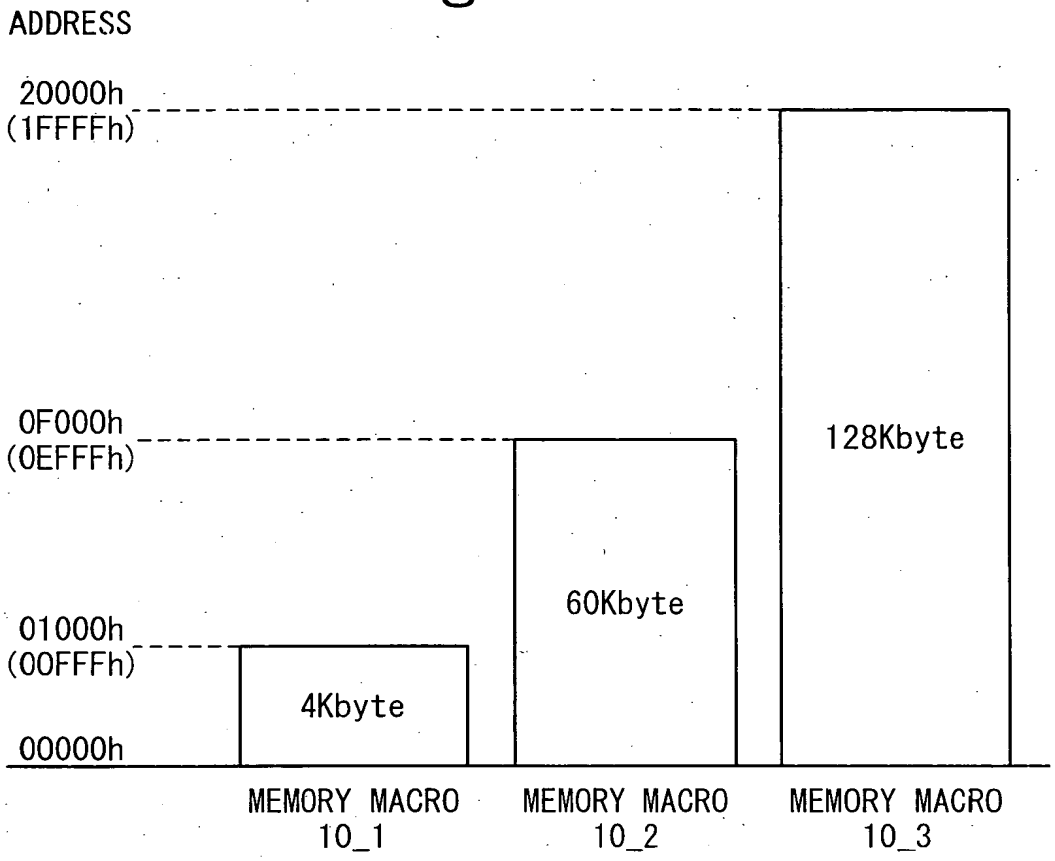


Fig. 10B

ADDRESS	00000h ～00FFFh	01000h ～0EFFFh	0F000h ～1FFFFh
TCES4_1	1	0	0
TCES4_2	1	1	0
TCES4_3	1	1	1

Fig. 11

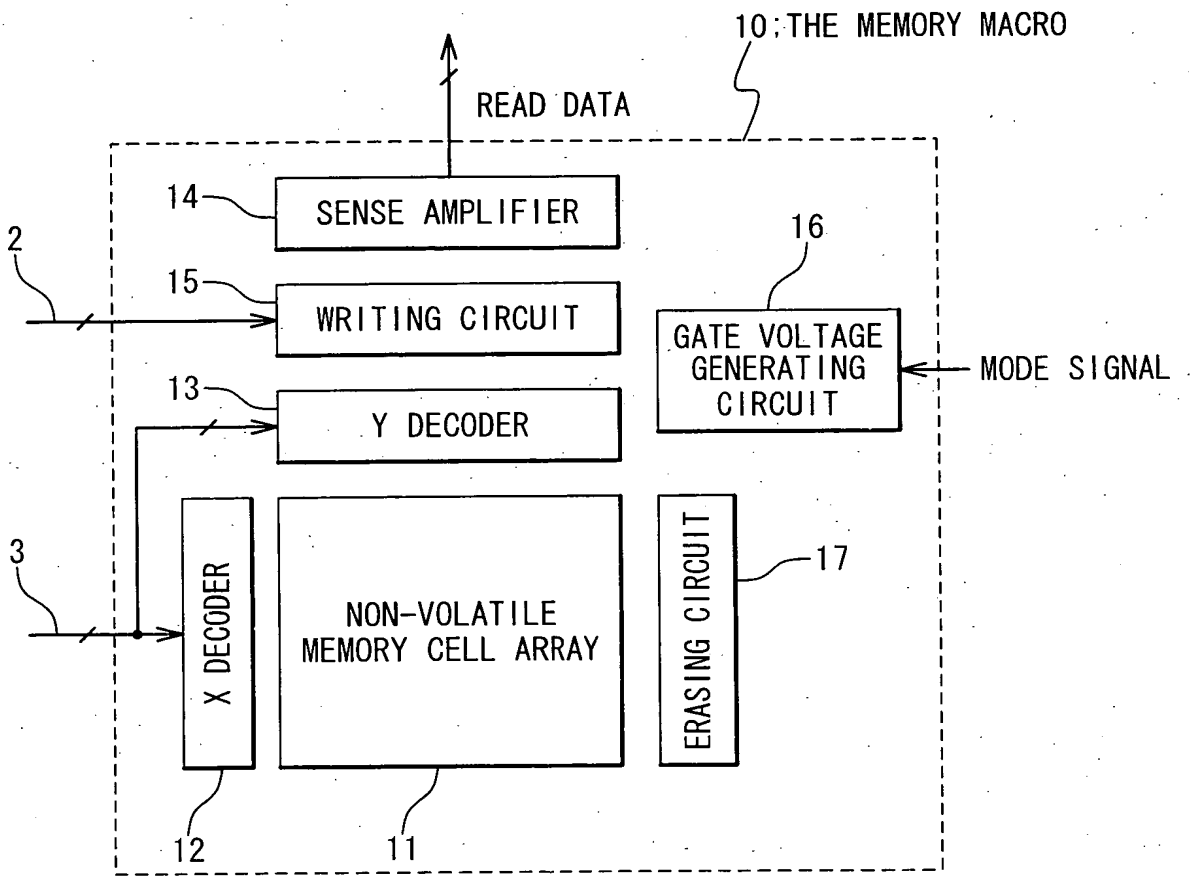

10:THE MEMORY MACRO
READ DATA
14
SENSE AMPLIFIER
2
15
WRITING CIRCUIT
16
GATE VOLTAGE GENERATING CIRCUIT
MODE SIGNAL
13
Y DECODER
3
X DECODER
NON-VOLATILE MEMORY CELL ARRAY
ERASING CIRCUIT
17
12
11

Fig. 12A

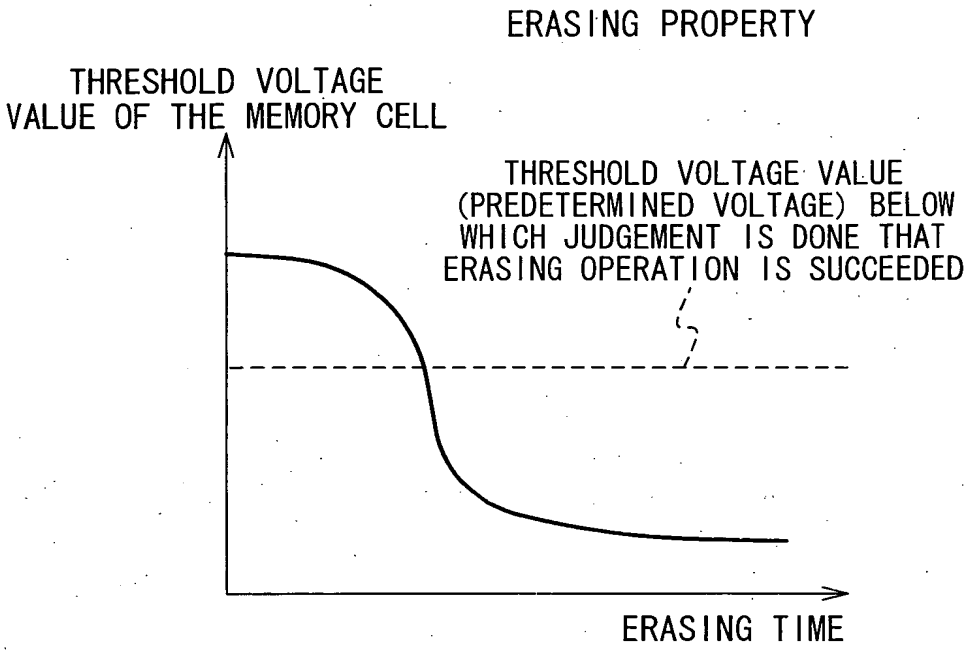


Fig. 12B

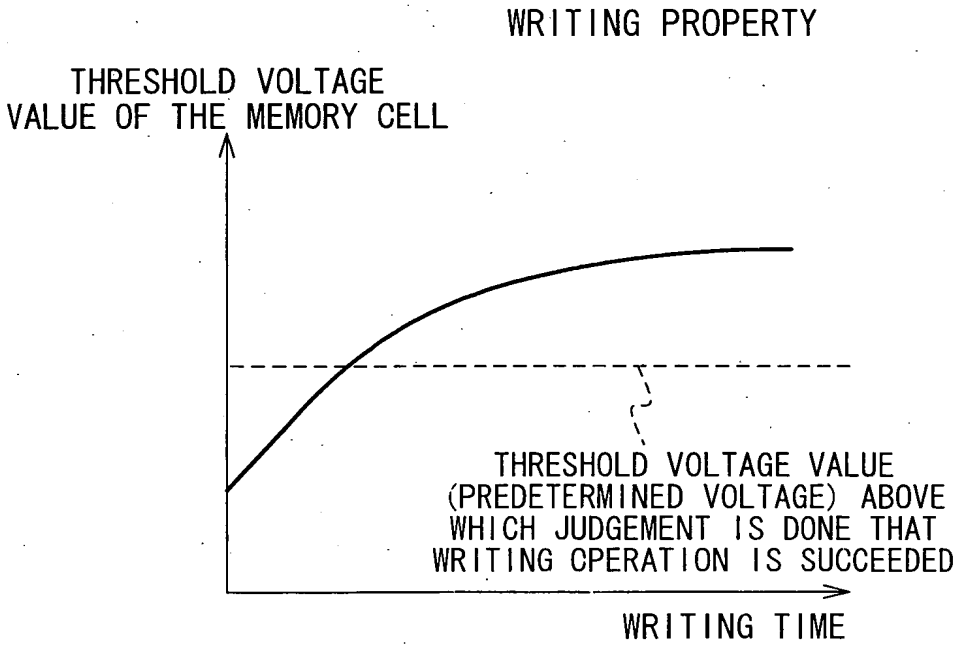


Fig. 13

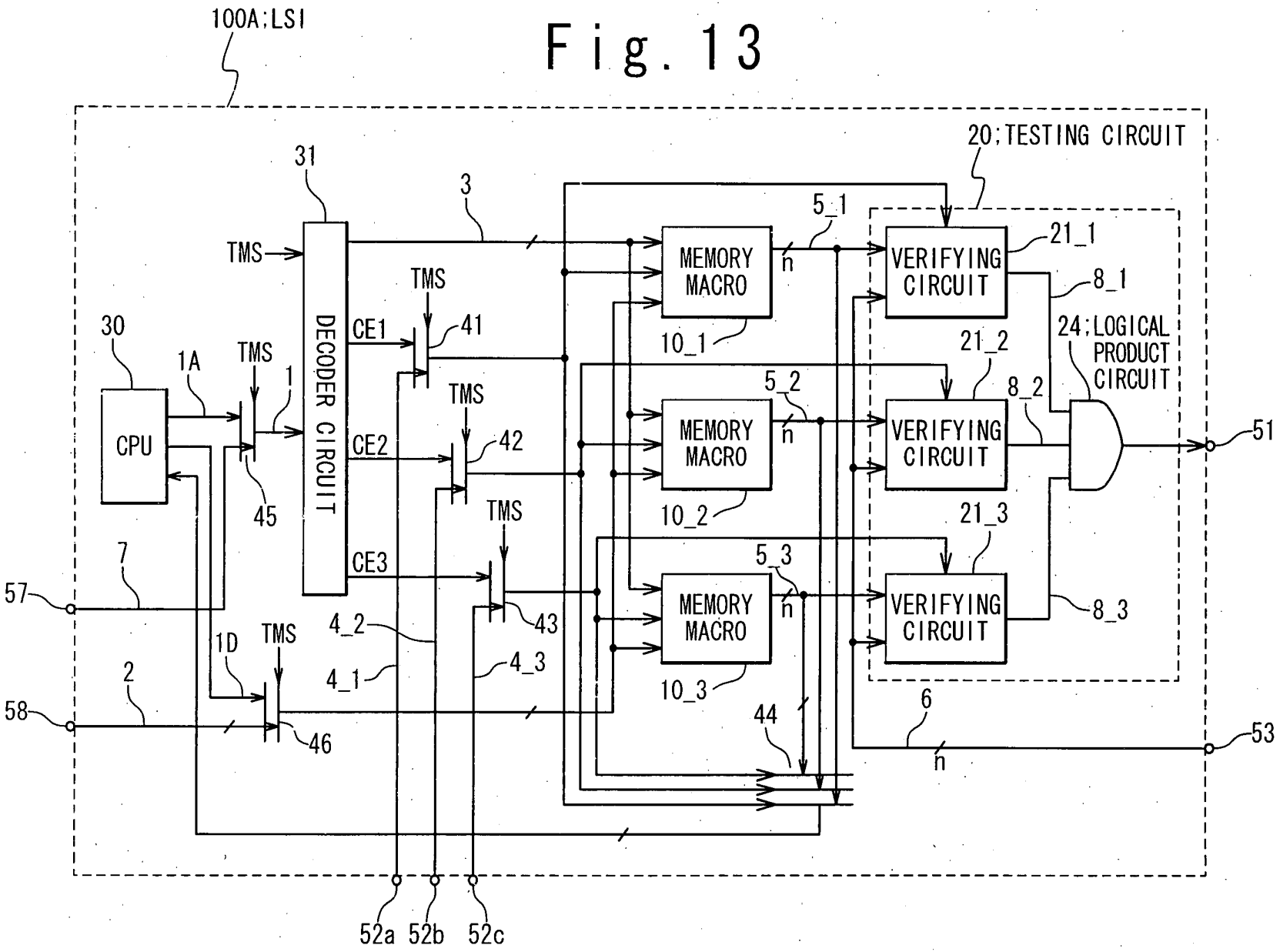

100A;LSI
20;TESTING CIRCUIT
31
3
TMS
DECODER CIRCUIT
CE1
CE2
CE3
30
CPU
1A
1
45
41
42
43
7
57
1D
2
58
46
4_1
4_2
4_3
MEMORY MACRO
10_1
10_2
10_3
5_1
5_2
5_3
n
VERIFYING CIRCUIT
21_1
21_2
21_3
8_1
8_2
8_3
24;LOGICAL PRODUCT CIRCUIT
51
44
6
53
52a
52b
52c

Fig. 14

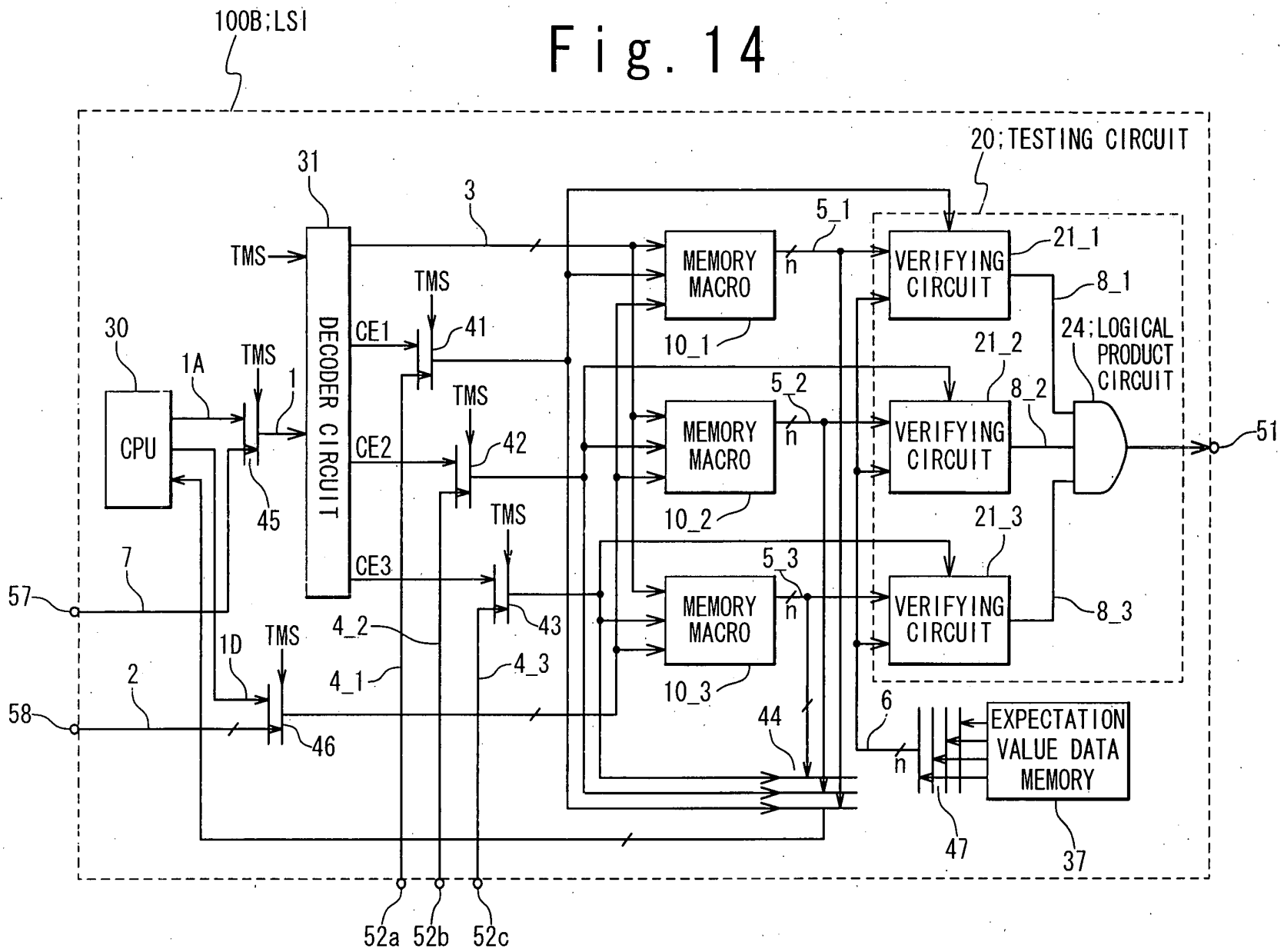

100B;LSI
20;TESTING CIRCUIT
31
3
TMS
DECODER CIRCUIT
CE1
CE2
CE3
41
42
43
30
CPU
1A
1
45
7
57
1D
2
58
46
4_1
4_2
4_3
MEMORY MACRO
10_1
10_2
10_3
5_1
5_2
5_3
n
VERIFYING CIRCUIT
21_1
21_2
21_3
8_1
8_2
8_3
24;LOGICAL PRODUCT CIRCUIT
51
44
6
EXPECTATION VALUE DATA MEMORY
47
37
52a
52b
52c

Fig. 15

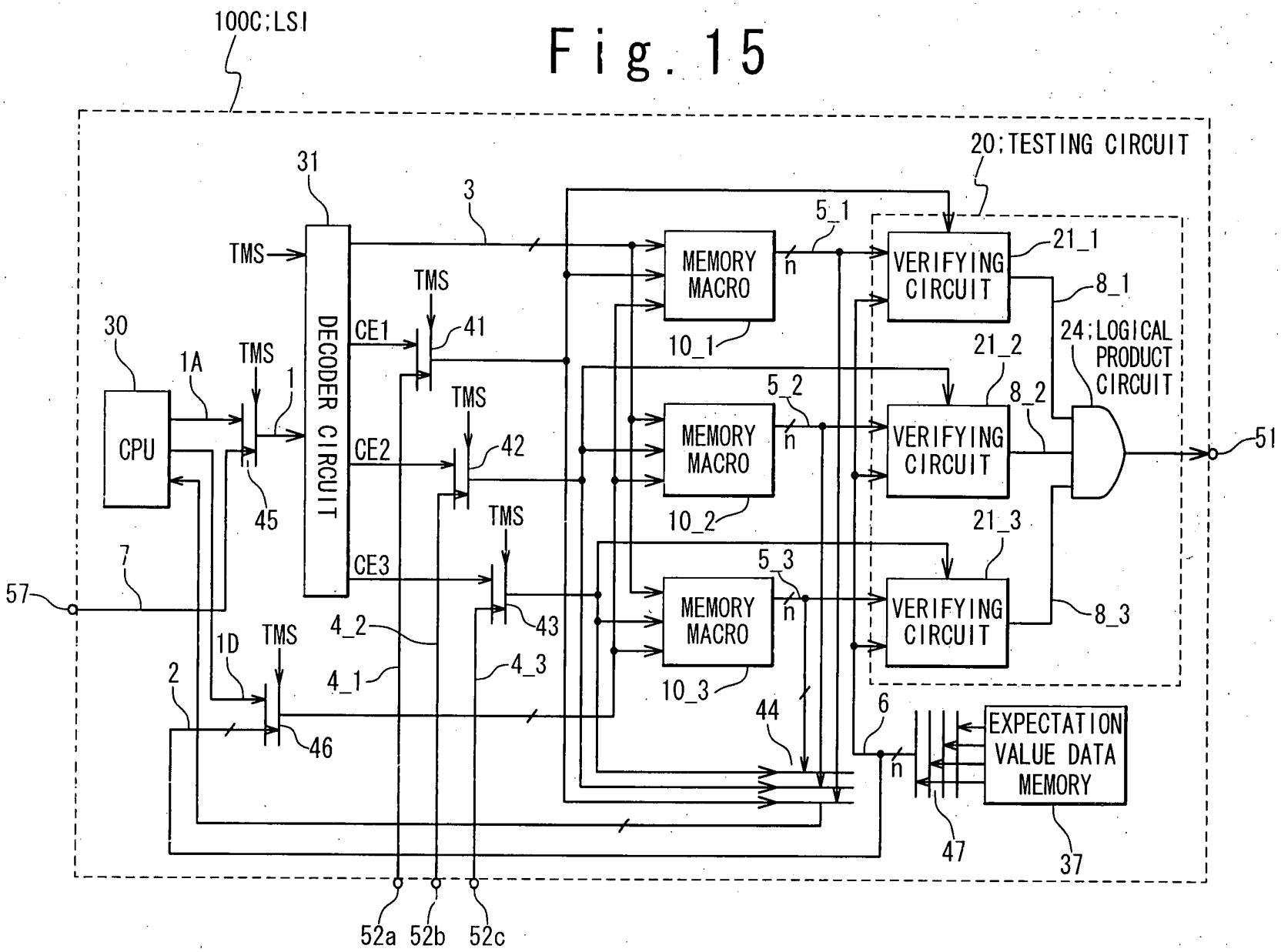
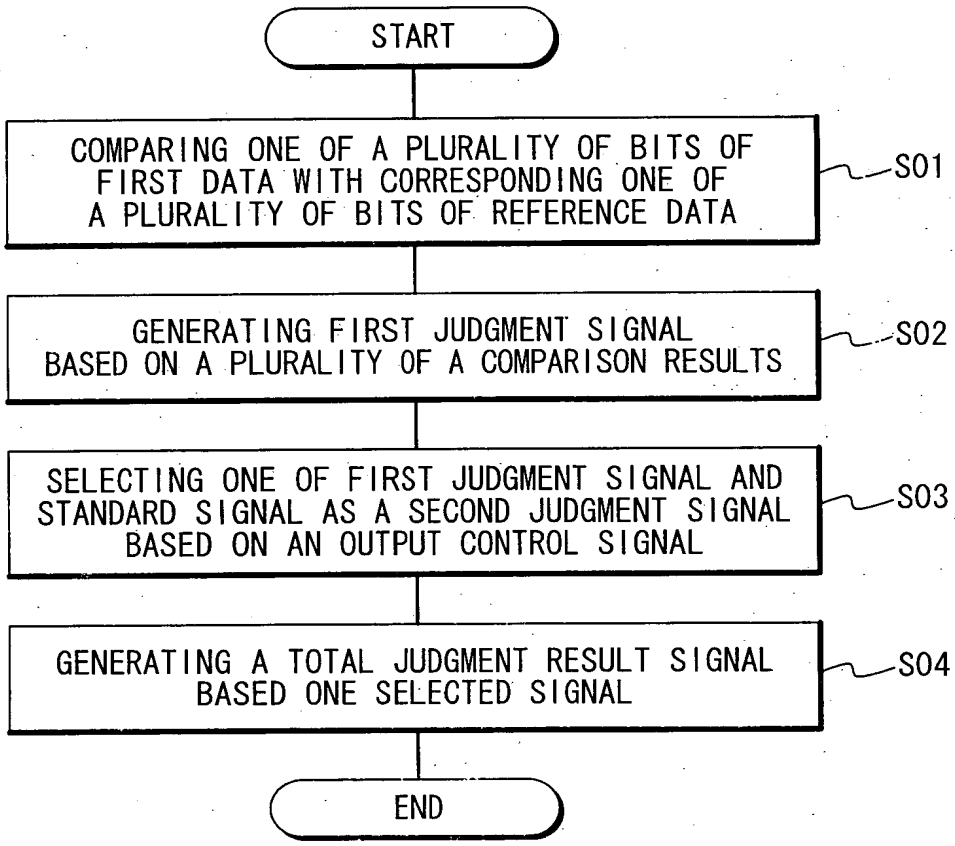

100C;LSI
20;TESTING CIRCUIT
31
3
TMS
DECODER CIRCUIT
CE1
CE2
CE3
41
42
43
30
CPU
1A
1
45
57
7
1D
2
46
4_1
4_2
4_3
MEMORY MACRO
10_1
10_2
10_3
5_1
5_2
5_3
n
VERIFYING CIRCUIT
21_1
21_2
21_3
8_1
8_2
8_3
24;LOGICAL PRODUCT CIRCUIT
51
44
6
EXPECTATION VALUE DATA MEMORY
37
47
52a
52b
52c

Fig. 16


START
COMPARING ONE OF A PLURALITY OF BITS OF FIRST DATA WITH CORRESPONDING ONE OF A PLURALITY OF BITS OF REFERENCE DATA
S01
GENERATING FIRST JUDGMENT SIGNAL BASED ON A PLURALITY OF A COMPARISON RESULTS
S02
SELECTING ONE OF FIRST JUDGMENT SIGNAL AND STANDARD SIGNAL AS A SECOND JUDGMENT SIGNAL BASED ON AN OUTPUT CONTROL SIGNAL
S03
GENERATING A TOTAL JUDGMENT RESULT SIGNAL BASED ONE SELECTED SIGNAL
S04
END